Decoding Algorithms in Iterative Decoding of Turbo Codes"). The rejections are respectfully traversed.

The Examiner asserts that the algorithm in Amon is executed in exactly three cycles. Notwithstanding the Examiner's contention that anyone of ordinary skill in the art at the time the invention was made or who was literate in the English language would make this interpretation, Applicant submits that col. 1, lines 18-31 of Amon should be interpreted in a very different way, an interpretation which is supported at several places in the Amon patent.

Applicant submits that col. 1, lines 18-31 of Amon should be interpreted as describing operations that occur in three different single clock cycles, but those *three single clock cycles are not consecutive clock cycles*. As a result of this interpretation, Amon does not read on Applicant's claims. This interpretation is supported as follows.

FIG. 4 of Amon illustrates a first embodiment of assembly code for implementing the ACS butterfly (col. 9, lines 24-36). As shown in FIG. 4, an add instruction and a load instruction appear in the second code line of the main ACS loop; a subtract instruction appears in the third code line of the main ACS loop; and compare (MAX) and refetch instructions appear in the fourth code line of the main ACS loop. It is well established that assembly code is written with parallel operations in the same code line and sequential operations in sequential code lines. Thus, the add, subtract and compare instructions are performed sequentially in different clock cycles. This interpretation is supported at col. 9, lines 30 and 31, where it is stated that one loop of the ACS butterfly is completed in 14 clock cycles. A loop execution time of 14 clock cycles is inconsistent with performing each of two instances of add, subtract and compare operations in a single clock cycle.

FIG. 5 illustrates a second embodiment of assembly code for implementing the ACS butterfly (col. 9, lines 37-49). Similarly to FIG. 4, add, subtract and compare instructions appear on second, third and fourth code lines, respectively of the main ACS loop. Amon states at col. 9, lines 45-46 that the assembly code of FIG. 5 permits one loop of the ACS butterfly to be performed in 10

clock cycles. Again, a loop execution time of 10 clock cycles is inconsistent with performing each of two instances of add, subtract and compare operations in a single clock cycle.

Claim 7 of the Amon patent corresponds generally with the language at col. 1, lines 18-31. Claim 11 recites steps of: (a) fetching during a first single clock cycle; (b) fetching during a second single clock cycle; (c) adding; (d) subtracting; (e) comparing, selecting and refetching during a third single clock cycle; (f) storing; etc. The adding, subtracting and comparing steps appear in separate paragraphs of claim 7. This is fully consistent with the assembly code shown in FIGs. 4 and 5 and with the interpretation that the first, second and third single clock cycles recited in these claims are not consecutive clock cycles. Applicant submits that one of ordinary skill in the art would read claim 7 of Amon, as well as the remainder of Amon, as requiring the comparing, selecting and refetching operations of step (e) to be performed in a single clock cycle and not as requiring the operations of steps (c), (d) and (e) to be performed in a single clock cycle. The claim language describes operations that occur during three single clock cycles which are not consecutive clock cycles.

In summary, Amon does not teach or suggest a method for processing signal values in a digital signal processor wherein *adding, subtracting, comparing and selecting operations of a single trellis instruction are executed by the digital signal processor in a single clock cycle*, as recited in Applicant's claims 1 and 18. In fact, Amon teaches to the contrary as explained above. Amon teaches separate add, subtract and compare instructions which are executed on different clock cycles. Accordingly, claims 1 and 18 are clearly and patentably distinguished over Amon, and withdrawal of the rejection is respectfully requested.

Claims 2-6 depend from claim 1, and claims 25 and 26 depend from claim 18. Claims 2-6, 25 and 26 are patentable over Amon for at least the same reasons as claims 1 and 18.

Based on the above discussion, claims 1-6, 18, 25 and 26 are in condition for allowance.

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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x08/23/2006

Respectfully submitted,

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